CLAIMS

1. A memory circuit comprising:

(1) a node for serially providing data read out of memory cells;

(2) circuitry comprising M stages S_1, ... S_M, where M>1, for holding sets of N data bits (D_0, D_1, ... D_{N-1}) read out of memory cells before serially providing the data bits to said node in the order D_0, D_1, ..., D_{N-1}, where $N \geq 2$, wherein each set of N data bits is read out of the memory cells in parallel, wherein each stage S_i ($i < M$) has at least N outputs for providing each set in parallel;

(3) a clock signal generator for generating one or more first clock signals and one or more second clock signals, wherein:

the stage S_{M-1} is responsive to one or more of the first clock signals to provide the data bit D_0 of each set to said node;

wherein the stage S_M is responsive to the one or more second clock signals for serially providing the bits D_1, ... D_{N-1} to said node;

wherein the one or more first clock signals are not a function of any second clock signal.

2. The memory circuit of Claim 1 wherein each stage S_i ($i < M$) is responsive to one or more of the first clock signals to provide the N data bits of each set in parallel on the stage's outputs.

3. The memory circuit of Claim 1 wherein each stage S_i ($i < M$) has at least N inputs for receiving each set in parallel, wherein the stage S_M is to receive in parallel N-1 bits of each set but is not to receive the bit D_0.

4. The memory circuit of Claim 1 wherein each stage S_i ($i > 1$) is to receive the bits of each set from the stage S_{i-1}.

5. The memory circuit of Claim 1 wherein $N \geq 4$.

6. The memory circuit of Claim 1 further comprising a circuit for specifying a variable latency between receipt of a read command by the memory and a serial output

of read data by the memory, wherein at least one of the first clock signals and at least one of the second clock signals are functions of the latency.

7. The memory circuit of Claim 1 wherein the stage S_1 comprises storage to hold at least two sets of N data bits, each set being read out of the memory cells in parallel, the two sets being read out of the memory cells at different times not in parallel with each other.

8. The memory circuit of Claim 1 further comprising N lines $L_0, L_1, \ldots L_{N-1}$ for carrying the N data bits of each set in parallel to the stage S_1, each line L_i (i=0, ..., N-1) carrying the respective data bit D_i of the set.

9. The memory circuit of Claim 1 further comprising:

N lines $L_0, L_1, \ldots L_{N-1}$ for carrying the N data bits of each set in parallel to the stage S_1;

circuitry for specifying an order in which the bits on the lines $L_0, L_1, \ldots L_{N-1}$ are to be provided on said node;

wherein the stages comprise circuitry for ordering the bits in said order.

10. A method for reading data from a memory, the method comprising:

(1) reading a set of N data bits ($D_0, D_1, \ldots D_{N-1}$) from memory cells in parallel, and loading the set of bits in parallel into a stage S_{M-1}, where $N \geq 2$;

(2) transferring the data bits ($D_0, D_1, \ldots D_{N-1}$) in parallel responsively to one or more first clock signals from the stage S_{M-1}, with the bit D_0 being transferred to a node for serially providing the data bits, and with the bits ($D_1, \ldots D_{N-1}$) being transferred to a stage S_M;

(3) after the operation (2), serially transferring the data bits ($D_1, \ldots D_{N-1}$) from the stage S_M to the node D responsively to one or more second clock signals;

wherein the one or more first clock signals are not a function of any second clock signal.

11. The method of Claim 10 further comprising specifying a variable latency between receipt of a read command by the memory and a serial output of the data bits (D_0, D_1, ... D_{N-1}) by the memory, wherein at least one of the first clock signals and at least one of the second clock signals are functions of the latency.

12. The method of Claim 11 wherein $N \geq 4$.

13. A memory circuit comprising:

(1) an input/output terminal;

(2) circuitry comprising M stages S_1, ... S_M, where M>1, for holding sets of N data bits (D_0, D_1, ... D_{N-1}) read out of memory cells before serially providing the data bits to said terminal in the order D_0, D_1, ..., D_{N-1}, where $N \geq 2$, wherein each set of N data bits is read out of the memory cells in parallel, wherein each stage S_i ($i < M$) has at least N outputs for providing each set in parallel;

(3) a clock signal generator for generating one or more first clock signals and one or more second clock signals, wherein:

the stage S_{M-1} is responsive to one or more of the first clock signals to provide the data bit D_0 of each set to said terminal;

wherein the stage S_M is responsive to the one or more second clock signals for serially providing the bits D_1, ... D_{N-1} to said terminal.

14. The memory circuit of Claim 13 wherein each stage S_i ($i < M$) is responsive to one or more of the first clock signals to provide the N data bits of each set in parallel on the stage's outputs, wherein the stage S_{M-1} is responsive to one or more of the first clock signals to provide the data bit D_0 of each set to said terminal;

15. The memory circuit of Claim 13 wherein each stage S_i ($i < M$) has at least N inputs for receiving each set in parallel, wherein the stage S_M is to receive in parallel N-1 bits of each set but is not to receive the bit D_0.

16. The memory circuit of Claim 13 wherein each stage S_i ($i > 1$) is to receive the bits of each set from the stage S_{i-1}.

17. The memory circuit of Claim 13 wherein $N \geq 4$.

18. The memory circuit of Claim 13 further comprising a circuit for specifying a variable latency between receipt of a read command by the memory and a serial output of read data by the memory, wherein at least one of the first clock signals and at least one of the second clock signals are functions of the latency.

19. The memory circuit of Claim 13 wherein the stage S_1 comprises storage to hold at least two sets of N data bits, each set being read out of the memory cells in parallel, the two sets being read out of the memory cells at different times not in parallel with each other.

20. The memory circuit of Claim 13 further comprising N lines $L_0, L_1, \ldots L_{N-1}$ for carrying the N data bits of each set in parallel to the stage S_1, each line L_i (i=0, ..., N-1) carrying the respective data bit D_i of the set.

21. The memory circuit of Claim 13 further comprising:

N lines $L_0, L_1, \ldots L_{N-1}$ for carrying the N data bits of each set in parallel to the stage S_1;

circuitry for specifying an order in which the bits on the lines $L_0, L_1, \ldots L_{N-1}$ are to be provided on said terminal;

wherein the stages comprise circuitry for ordering the bits in said order.